74HC107; 74HCT107

Dual JK flip-flop with reset; negative-edge trigger

Rev. 4 — 26 January 2015 Product data sheet

1. General description

The 74HC107; 74HCT107 is a dual negative edge triggered JK flip-flop featuring individual J and K inputs, clock ($\overline{CP}$) and reset ($\overline{R}$) inputs and complementary Q and $\overline{Q}$ outputs. The reset is an asynchronous active LOW input and operates independently of the clock input. The J and K inputs control the state changes of the flip-flops as described in the mode select function table. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Complies with JEDEC standard no. 7A
- Input levels:
  - The 74HC107: CMOS levels
  - The 74HCT107: TTL levels
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC107N	–40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HCT107N				
74HC107D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT107D				
74HC107DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HC107PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram

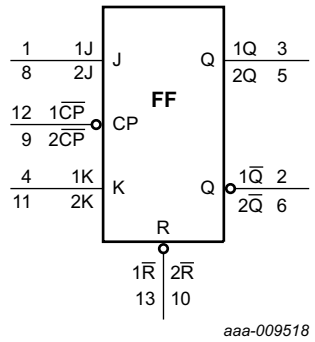


Fig 1. Logic symbol

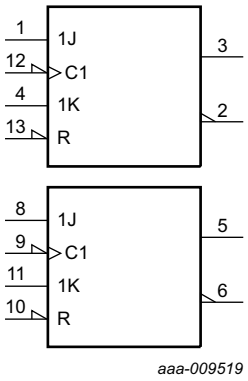


Fig 2. IEC logic symbol

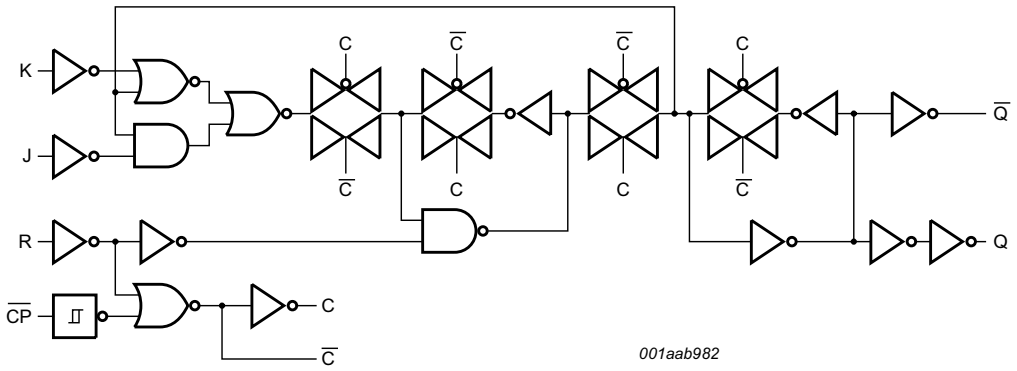


Fig 3. Logic diagram (one flip-flop)

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5. Pinning information

5.1 Pinning

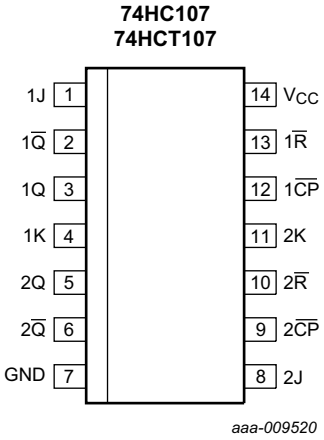


Fig 4. Pin configuration DIP14, SO14 and (T)SSOP14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1J, 2J	1, 8	synchronous J input
$1\overline{Q}$, $2\overline{Q}$	2, 6	complement output
1Q, 2Q	3, 5	true output
1K, 2K	4, 11	synchronous K input
$1\overline{CP}$, $2\overline{CP}$	12, 9	clock input (HIGH-to-LOW edge-triggered)
$1\overline{R}$, $2\overline{R}$	13, 10	asynchronous reset input (active LOW)
GND	7	ground (0 V)
V_{CC}	14	supply voltage

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6. Functional description

Table 3. Function table[1]

Input				Output		Operating mode
$\overline{R}$	$\overline{CP}$	J	K	Q	$\overline{Q}$	
L	X	X	X	L	H	asynchronous reset
H	↓	h	h	$\overline{q}$	q	toggle
H	↓	l	h	L	H	load 0 (reset)
H	↓	h	l	H	L	load 1 (set)
H	↓	l	l	q	$\overline{q}$	hold (no change)

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW clock transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the HIGH-to-LOW clock transition;
q = state of referenced output one set-up time prior to the HIGH-to-LOW clock transition;
X = don't care;
↓ = HIGH-to-LOW clock transition.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V [1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V [1]	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V	-	±25	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		−50	-	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
		DIP14 package [2]	-	750	mW
		SO14 package [3]	-	500	mW
		(T)SSOP14 package [4]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 12 mW/K above 70 °C.

[3] P_{tot} derates linearly with 8 mW/K above 70 °C.

[4] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC107			74HCT107			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC107										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	4.0	-	40	-	80	μA

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Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_I	input capacitance		-	3.5	-					pF
74HCT107										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = –20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 μA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} – 2.1 V; I_O = 0 A; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V								
		pin n$\overline{CP}$, nJ	-	100	360	-	450	-	490	μA
		pin n$\overline{R}$	-	65	234	-	293	-	319	μA
		pin nK	-	60	216	-	270	-	294	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

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10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 7

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC107										
t_{pd}	propagation delay	$n\overline{CP}$ to nQ; see Figure 5 [1]								
		V_{CC} = 2.0 V	-	52	160	-	200	-	240	ns
		V_{CC} = 4.5 V	-	19	32	-	40	-	48	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	15	27	-	34	-	41	ns
		$n\overline{CP}$ to $n\overline{Q}$; see Figure 5								
		V_{CC} = 2.0 V	-	52	160	-	200	-	240	ns
		V_{CC} = 4.5 V	-	19	32	-	40	-	48	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	15	27	-	34	-	41	ns
		$n\overline{R}$ to nQ, $n\overline{Q}$; see Figure 6								
		V_{CC} = 2.0 V	-	52	155	-	195	-	235	ns
		V_{CC} = 4.5 V	-	19	31	-	39	-	47	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	15	26	-	33	-	40	ns
t_t	transition time	nQ, $n\overline{Q}$; see Figure 5 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	$n\overline{CP}$ input, HIGH or LOW; see Figure 5								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		$n\overline{R}$ input, HIGH or LOW; see Figure 6								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t_{rec}	recovery time	$n\overline{R}$ to $n\overline{CP}$; see Figure 6								
		V_{CC} = 2.0 V	60	19	-	75	-	90	-	ns
		V_{CC} = 4.5 V	12	7	-	15	-	18	-	ns
		V_{CC} = 6.0 V	20	6	-	13	-	15	-	ns
t_{su}	set-up time	nJ, nK to $n\overline{CP}$; see Figure 5								
		V_{CC} = 2.0 V	100	22	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	8	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	6	-	21	-	26	-	ns

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Table 7. Dynamic characteristics *...continued*

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 7

Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_h	hold time	nJ, nK to $n\overline{CP}$; see Figure 5								
		V_{CC} = 2.0 V	3	–6	-	3	-	3	-	ns
		V_{CC} = 4.5 V	3	–2	-	3	-	3	-	ns
		V_{CC} = 6.0 V	3	–2	-	3	-	3	-	ns
f_{max}	maximum frequency	$n\overline{CP}$ input; see Figure 5								
		V_{CC} = 2.0 V	6	23	-	4.8	-	4.0	-	MHz
		V_{CC} = 4.5 V	30	70	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	78	-	-	-	-	-	MHz
		V_{CC} = 6.0 V	35	85	-	28	-	24	-	MHz
C_{PD}	power dissipation capacitance	per flip-flop; [3] V_I = GND to V_{CC}	-	30	-	-	-	-	-	pF
74HCT107										
t_{pd}	propagation delay	$n\overline{CP}$ to nQ; see Figure 5 [1]								
		V_{CC} = 4.5 V	-	19	36	-	45	-	54	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	16	-	-	-	-	-	ns
		$n\overline{CP}$ to $n\overline{Q}$; see Figure 5								
		V_{CC} = 4.5 V	-	21	36	-	45	-	54	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	18	-	-	-	-	-	ns
		$n\overline{R}$ to nQ, $n\overline{Q}$; see Figure 6								
		V_{CC} = 4.5 V	-	20	38	-	48	-	57	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	17	-	-	-	-	-	ns
t_t	transition time	nQ, $n\overline{Q}$; see Figure 5 [2]								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t_W	pulse width	$n\overline{CP}$ input, HIGH or LOW; see Figure 5								
		V_{CC} = 4.5 V	16	9	-	20	-	24	-	ns
		$n\overline{R}$ input, HIGH or LOW; see Figure 6								
		V_{CC} = 4.5 V	20	11	-	25	-	30	-	ns
t_{rec}	recovery time	$n\overline{R}$ to $n\overline{CP}$; see Figure 6								
		V_{CC} = 4.5 V	14	8	-	18	-	21	-	ns
t_{su}	set-up time	nJ, nK to $n\overline{CP}$; see Figure 5								
		V_{CC} = 4.5 V	20	7	-	25	-	30	-	ns
t_h	hold time	nJ, nK to $n\overline{CP}$; see Figure 5								
		V_{CC} = 4.5 V	5	–2	-	5	-	5	-	ns

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Table 7. Dynamic characteristics *...continued*

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Figure 7

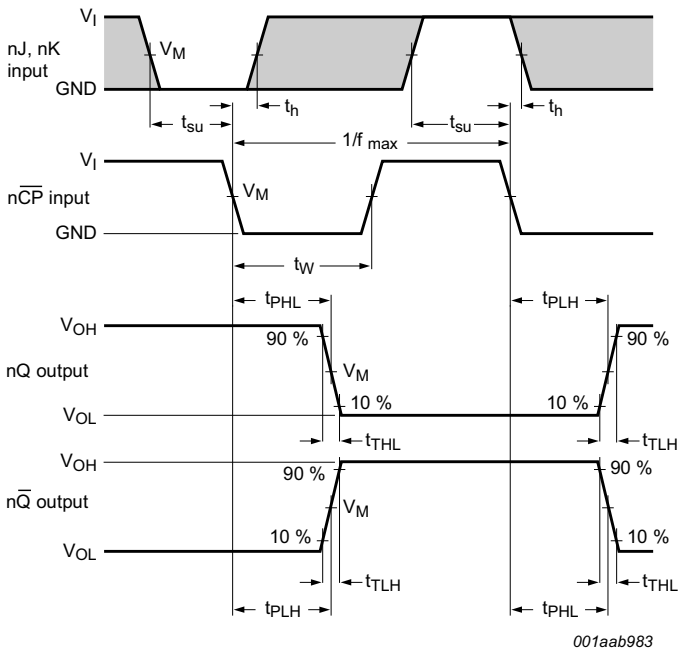
Symbol	Parameter	Conditions	25 °C			–40 °C to +85 °C		–40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	maximum frequency	$n\overline{CP}$ input; see Figure 5								
		V_{CC} = 4.5 V	30	66	-	24	-	20	-	MHz
		V_{CC} = 5.0 V; C_L = 15 pF	-	73	-	-	-	-	-	MHz
C_{PD}	power dissipation capacitance	per flip-flop; [3] V_I = GND to V_{CC} − 1.5 V	-	30	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.

[2] t_t is the same as t_{THL}, t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



The shaded areas indicate when the input is permitted to change for predictable output performance.

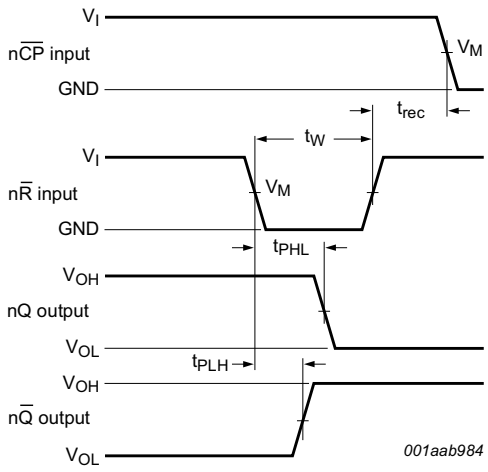
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Clock propagation delays, pulse width, set-up and hold times, output transition times and the maximum frequency

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Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

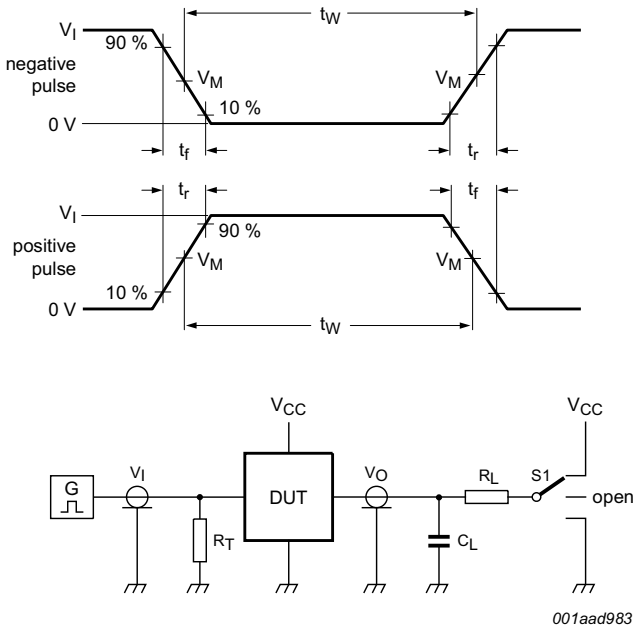
Fig 6. Reset propagation delays, pulse width and recovery time

Table 8. Measurement points

Type	Input		Output
	V_I	V_M	V_M
74HC107	V_{CC}	$0.5V_{CC}$	$0.5V_{CC}$
74HCT107	3 V	1.3 V	1.3 V

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Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig 7. Test circuit for measuring switching times

Table 9. Test data

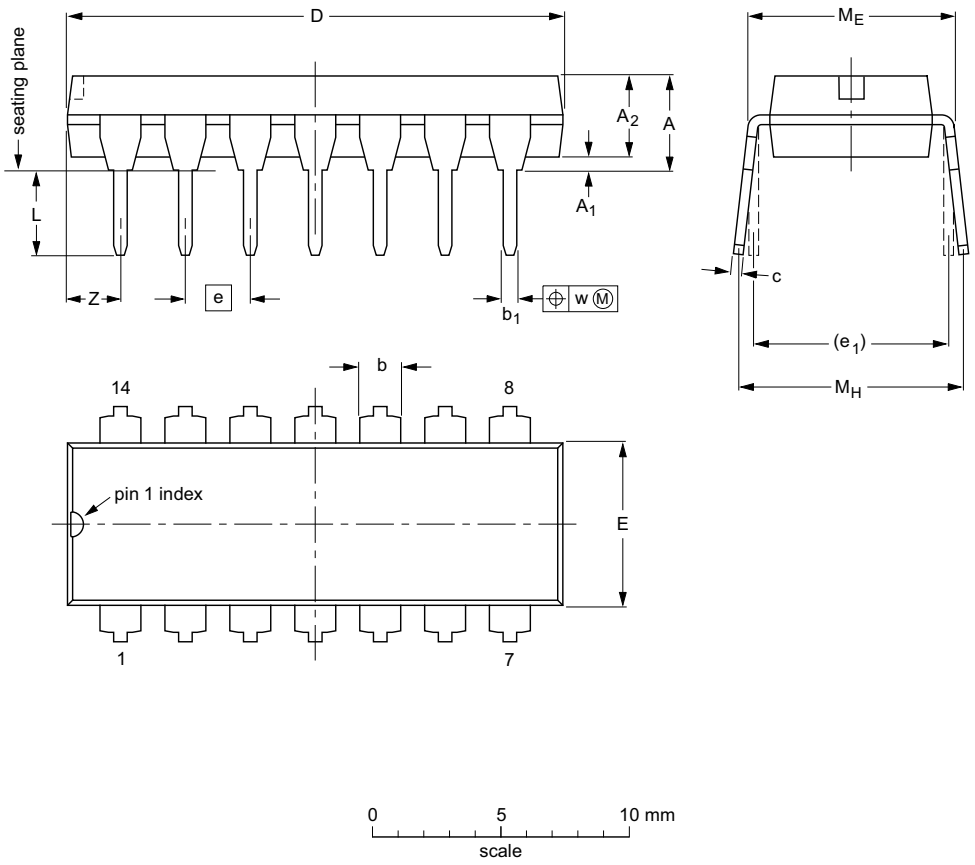
Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC107	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74HCT107	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

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12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

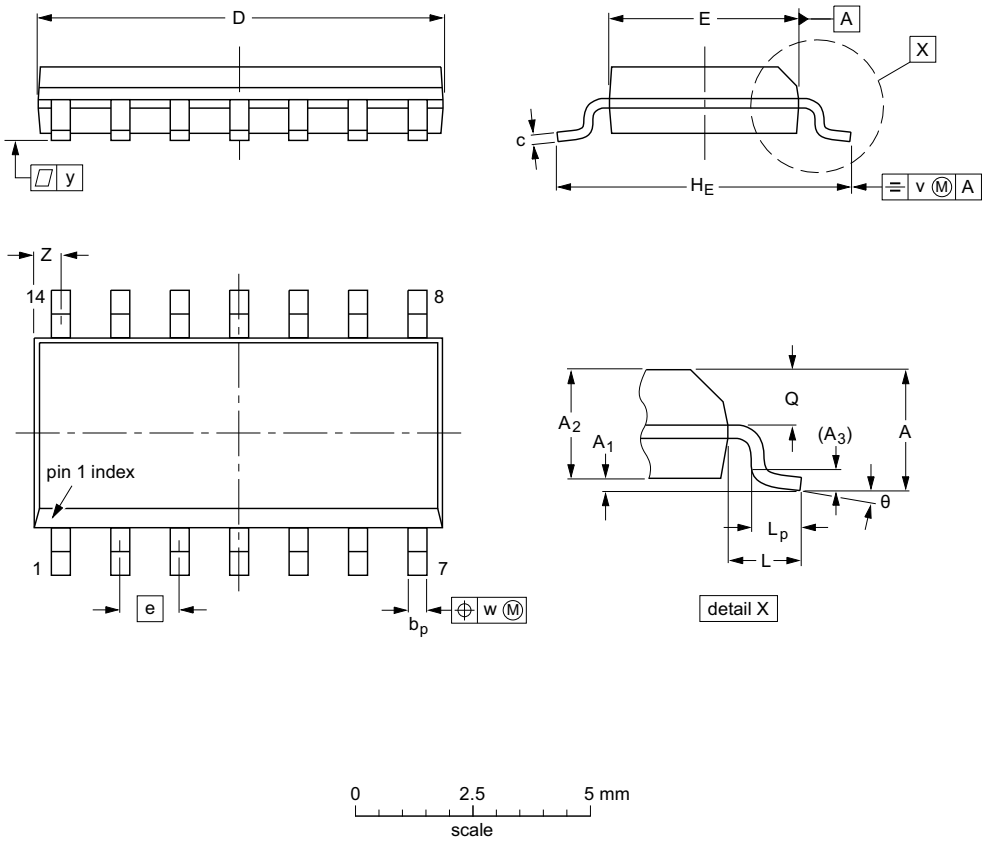
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 8. Package outline SOT27-1 (DIP14)

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SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

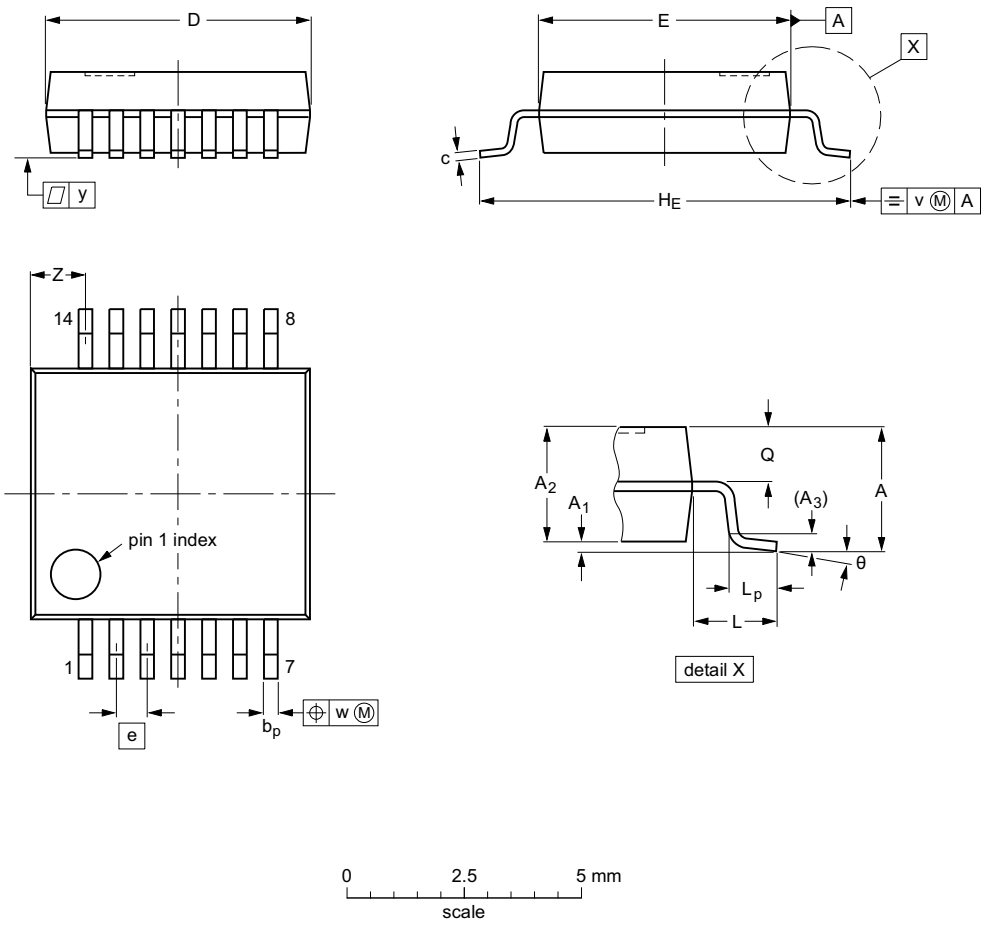
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT108-1 (SO14)

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SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

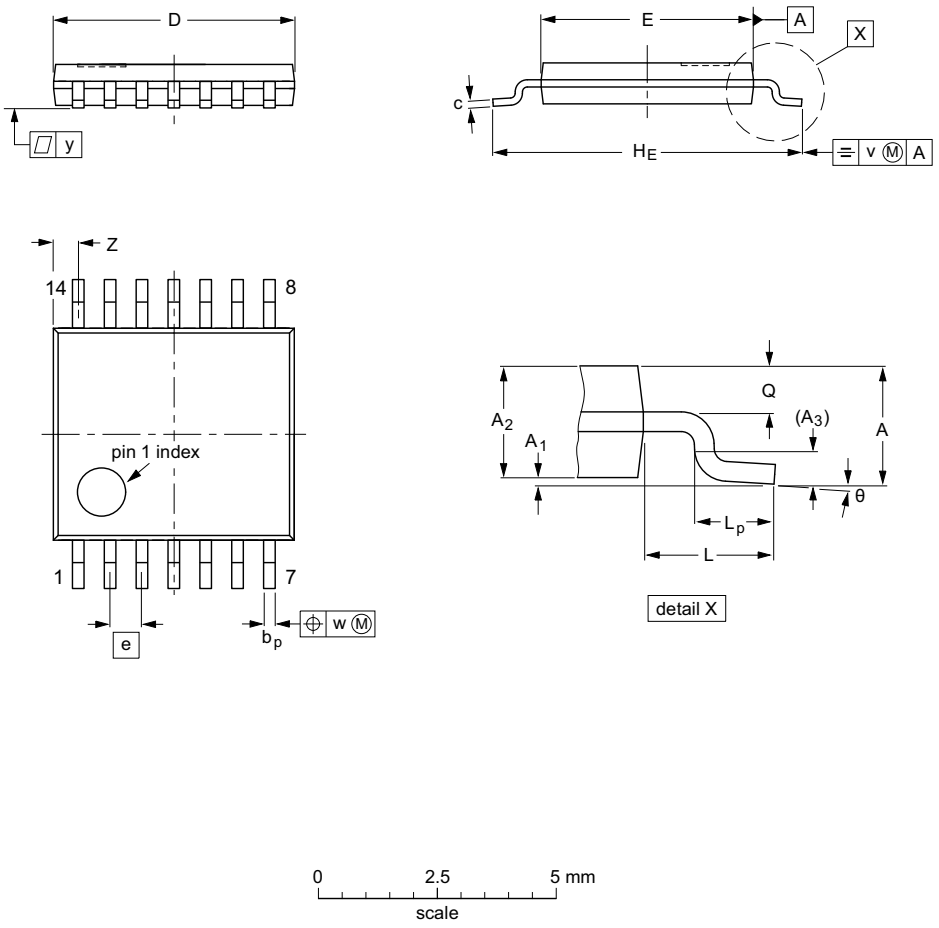
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT337-1 (SSOP14)

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TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 11. Package outline SOT402-1 (TSSOP14)

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13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charge-Device Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT107 v.4	20150126	Product data sheet	-	74HC_HCT107 v.3
Modifications:	• Table 7: Power dissipation capacitance condition for 74HCT107 is corrected.			
74HC_HCT107 v.3	20131118	Product data sheet	-	74HC_HCT107_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT107_CNV v.2	19901201	Product specification	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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